WHAT IS CLAIMED IS:

1. A system comprising:

a bus; and

an agent coupled to said bus and to receive a clock signal for said bus, said clock signal having a rising edge and a falling edge during use, wherein said agent is configured to drive one or more signals on said bus responsive to a first edge of said rising edge or said falling edge, and wherein said agent is configured to sample a value on said bus responsive to a second edge of said rising edge or said falling edge.

2. The system as recited in claim 1 wherein said first edge is said rising edge and said second edge is said falling edge.

3. The system as recited in claim 1 wherein said first edge is said falling edge and said second edge is said rising edge.

4. The system as recited in claim 1 wherein said agent is configured to terminate driving said one or more signals responsive to said second edge.

5. The system as recited in claim 4 wherein said agent is configured to precharge said one or more signals during a period of time between an occurrence of said second edge and a subsequent occurrence of said first edge.

6. The system as recited in claim 1 wherein said agent is configured to evaluate said value to determine if said agent is to drive said one or more signals responsive to said

second edge, and wherein said agent is configured to drive said one or more signals on a next occurrence of said first edge responsive to evaluating said value.

7. The system as recited in claim 1 wherein said bus comprises a differential pair of conductors for a first signal.

8. The system as recited in claim 7 wherein said agent is configured to drive one of said differential pair to drive said first signal responsive to a first value to be driven on said first signal.

9. The system as recited in claim 8 wherein said agent is configured to drive said one of said differential pair low.

10. The system as recited in claim 1 wherein said bus comprises an address bus, a data bus, and response lines, and wherein said response lines carry signals to maintain cache coherency with respect to transactions on said bus, and wherein a transmission of data corresponding to two or more transactions on said data bus is capable of occurring out of order with respect to a transmission of addresses corresponding to said two or more transactions on said address bus.

11. The system as recited in claim 10 wherein transmission of a response corresponding to a first transaction on said response lines of said bus is fixed in time with respect to transmission of an address corresponding to said first transaction on said address bus.

12. A method comprising:

driving a value on a bus responsive to a first edge of a rising edge or a falling edge of a clock signal for said bus; and

sampling said value from said bus responsive to a second edge of said rising edge or said falling edge.

13. The method as recited in claim 12 wherein said first edge is said rising edge and said second edge is said falling edge.

14. The method as recited in claim 12 wherein said first edge is said falling edge and said second edge is said rising edge.

15. The method as recited in claim 12 further comprising terminating said driving said value responsive to said second edge.

16. The method as recited in claim 15 further comprising precharging said bus during a period of time between an occurrence of said second edge and a subsequent occurrence of said first edge.

17. The method as recited in claim 12 further comprising:

evaluating said value responsive to said second edge; and

driving a second value on a next occurrence of said first edge responsive to said evaluating said value.

18. The method as recited in claim 12 wherein said bus comprises a differential pair of conductors for a first signal.

19. The method as recited in claim 18 wherein said driving said value comprises driving

one of said differential pair to drive said first signal responsive to said value.

20. The method as recited in claim 19 wherein said driving said one of said differential pair comprises driving said one of said differential pair low.

21. The method as recited in claim 12 wherein said bus comprises an address bus, a data bus, and response lines, and wherein said response lines carry signals to maintain cache coherency with respect to transactions on said bus, and wherein a transmission of data corresponding to two or more transactions on said data bus is capable of occurring out of order with respect to a transmission of addresses corresponding to said two or more transactions on said address bus.

22. The method as recited in claim 21 wherein transmission of a response corresponding to a first transaction on said response lines of said bus is fixed in time with respect to transmission of an address corresponding to said first transaction on said address bus.